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FACSIMILE TRANSMITTAL SHEET

TO:	FROM:
Ms. Marcelli	Cathleen Stanton
DEPT:	DATE: September 15, 2004
COMPANY: US Patent & Trademark Office	FAX NUMBER: 845 471 2064
FAX NUMBER: 703 308 7333	PHONE NUMBER: 845 452 5863
RE: 09/821,546	# OF PAGES (INCLUDE THIS COVER): 14
NOTES/COMMENTS:	

Dear Ms. Marcelli,

As requested, please find attached the Office Action response of March 5, 2004 and the copy of the postcard with the PTO stamped date of March 8, 2004.

With Best Regards,

Cathleen Stanton

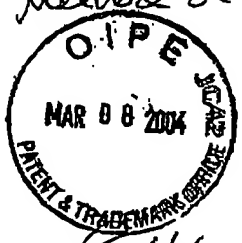
Cathleen Stanton

09/821,516 03/30/01 MEG-00-012
March 5, 2004

MAR. 1 4 2004

J.Y. Lee

A Structure and Manufacturing Method of Chip Scale Package



Response to Final Office Action
Faxed by PTO

MEG-00-012

March 4, 2004

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: Stephen B. Ackerman, Reg. No. 37,761
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject:

Serial No.	09/621,546	03/30/2001
J. Y. LEE		
"A STRUCTURE AND MANUFACTURING METHOD OF CHIP SCALE PACKAGE"		
Grp. Art Unit: 2811		D. W. OWENS

RESPONSE FINAL PATENT OFFICE ACTION

Dear Sir:

In response to the Office Action dated January 16, 2004, please amend the above-identified application for patent as follows:

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 5, 2004.

Rosemary L. S. Pike, Reg. No. 39,332

Signature Rosemary L. S. Pike

Date March 4, 2004

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Amendments to the Claims are reflected in the listing of the Claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 11 of this paper.

Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1-10. (canceled)

11. (previously presented) A method of forming a chip scale package (CSP) comprising the steps of:

providing one or more chips having I/O pads with UBM layer on the surface of said I/O pads;

providing a substrate comprising bismaleimide triazine (BT) and having a thickness between about 150 to 300 μm;

applying an adhesive layer with a thickness between about 10 to 100 μm over said substrate, thus forming an adsubstrate composite;

forming openings in said adsubstrate composite to match the spacing of corresponding said I/O pads of said chip;

attaching said chip(s) on said adsubstrate composite wherein said I/O pads of said chip(s) are placed on the corresponding openings on said adsubstrate composite to form a package;

forming a molding material around said package;

performing ball mounting over said openings on said adsubstrate of said package; and

sawing said substrate to form said CSP.

12. (original) The method of claim 11, wherein said chip comprises silicon.

13. (original) The method of claim 11, wherein said I/O pads are area array (AA) type, or are redistributed to a redistribution layer to form AA I/O pads.

14. (canceled)

15. (currently amended) The method of claim 11, wherein said substrate comprises a Ball Grid Array (BGA).

16. (canceled)

17. (original) The method of claim 11, wherein said adhesive layer comprises polyimide thermocompression advesive.

18. (canceled)

19. (original) The method of claim 11, wherein said forming said openings is accomplished by mechanical or laser drilling, or screen printing.

20. (original) The method of claim 11, wherein said openings have a diameter between about 350 to 900 μm.

21. (original) The method of claim 11, wherein said attaching said chip(s) is accomplished by subjecting said adsubstrate to a temperature between about 250 and 350 °C at a pressure between about 1.5 to 2.5 Mpascals.

22. (original) The method of claim 11, wherein said molding material comprises epoxy resin.

23. (original) The method of claim 11, wherein said molding material has a thickness between about 100 to 500 μm.

24. (original) The method of claim 11, wherein said performing said ball mounting is accomplished with a solder comprising tin-lead or tin-silver alloy.

25. (original) The method of claim 11, wherein said ball mountings have a height between about 300 to 800 μm.

26. (previously presented) A method of forming a chip scale package (CSP) comprising the steps of:

providing a wafer having a plurality of chip sites with I/O pads;

forming an under-ball metal (UBM) layer over said I/O pads;

forming an adhesive layer over said UBM layer on said wafer to form an adwafer;

forming openings in said adhesive layer on said adwafer to reach said I/O pads underlying said UBM layer;

thereafter die sawing said adwafer to form said chip scale package (CSP)

providing a substrate having openings corresponding to said I/O pads;

thereafter attaching said CSP with said adhesive to said substrate; and

thereafter forming ball mountings on said openings on said substrate to attach to said I/O pads on said CSP.

27. (original) The method of claim 26, wherein said wafer comprises silicon.

28. (original) The method of claim 26, wherein said I/O pads comprise aluminum alloy or copper.

29. (original) The method of claim 26, wherein said I/O pads are area array (AA) type, or redistributed to a redistribution layer to form AA pads.

30. (original) The method of claim 26, wherein said UBM layer comprises nickel and/or copper.

31. (original) The method of claim 26, wherein said forming said adhesive layer over said UBM layer comprises lamination, spin coating, or screen printing.

32. (original) The method of claim 26, wherein said adhesive layer comprises polyimide thermocompression advesive.

33. (canceled)

34. (original) The method of claim 26, wherein said forming said openings comprise laser drilling, photolithography, or silk screening.

35. (original) The method of claim 26, wherein said openings have a diameter between about 250 to 750 μm.

36. (original) The method of claim 26, wherein said substrate comprises bismaleimide trizine (BT) having a thickness between about 150 to 300 μm.

37. (currently amended) The method of claim 26, wherein said substrate comprises a Ball Grid Array (BGA).

38. (original) The method of claim 26, wherein said attaching said BGA substrate to said adhesive layer is accomplished at a temperature between about 250 and 350 °C, and pressure between about 1.5 to 2.5 Mpascals.

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39. (original) The method of claim 26, wherein said ball mountings comprise solder having a composition lead-tin or tin-silver.

40. (original) The method of claim 26, wherein said mounting balls have a height between about 300 to 800 μm.

41. (original) The method of claim 26, wherein said CSP is encapsulated in a molding material comprising epoxy resin.

42. (previously presented) A method of forming a chip scale package (CSP) comprising the steps of:

providing one or more chips having I/O pads with UBM layer on the surface of said I/O pads;

providing a substrate comprising bismaleimide triazine (BT) and having a thickness between 150 to 300 μm;

applying an adhesive layer with a thickness between 10 to 100 μm over said substrate, thus forming an adsubstrate composite;

forming openings in said adsubstrate composite to match the spacing of corresponding said I/O pads of said chip;

attaching said chip(s) on said adsubstrate composite wherein said I/O pads of said chip(s) are placed on the corresponding openings on said adsubstrate composite to form a package wherein said attaching is accomplished by subjecting said adsubstrate to a temperature of between 250 and 350 °C at a pressure of between 1.5 to 2.5 Mpascals;

forming a molding material around said package;

thereafter performing ball mounting over said openings on said adsubstrate of said package; and

sawing said substrate to form said CSP.

43. (previously presented) The method of claim 42 wherein said chip comprises silicon.

44. (previously presented) The method of claim 42 wherein said I/O pads are area array (AA) type, or are redistributed to a redistribution layer to form AA I/O pads.

45. (currently amended) The method of claim 42 wherein said substrate comprises a Ball Grid Array (BGA).

46. (previously presented) The method of claim 42 wherein said adhesive layer comprises polyimide thermocompression adhesive.

47. (previously presented) The method of claim 42 wherein said forming said openings is accomplished by mechanical or laser drilling or screen printing.

48. (previously presented) The method of claim 42 wherein said openings have a diameter between about 350 and 900 μm.

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49. (previously presented) The method of claim 42 wherein said molding material comprises epoxy resin.

50. (previously presented) The method of claim 42 wherein said performing said ball mounting is accomplished with a solder comprising tin-lead or tin-silver alloy.

51. (previously presented) The method of claim 42 wherein said ball mountings have a height between about 300 and 800 μm.

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REMARKS

Examiner D. Owens is thanked for the thorough examination and search of the subject Patent Application. Claims 15, 37, and 45 have been amended,

Claim 45 has been amended to overcome objection because of informalities as required by the Examiner. The same error has been corrected in Claims 15 and 37.

The Examiner is thanked for allowing Claims 26-32 and 34-41.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 11-13, 15, 17, 19, 20, and 22-25 as being unpatentable over Akram et al in view of Fanworth is requested in accordance with the following remarks.

In Applicants' invention, described on pages 9-12 and with reference to Figs. 2a-2i, an integrated circuit chip or chips 100 (Figs, 2a, 2aa, and 2b) are to be attached to substrate 150 (Fig. 2c). Substrate 150 is preferably BT mounted with an adhesive 160. These two pieces to be joined are claimed in Claim 11 in lines 2-3 (chip 100) and lines 5-8 (substrate 150 with adhesive 160). Now, via openings 170 are formed in the substrate (Claim 11, lines 9-10). Next, the chip is attached to the adsubstrate (lines 11-13, Fig. 2f). The claim language requires this order of steps – form via openings, then attach the chip to the adsubstrate wherein the I/O pads on the chip are placed on the openings on the adsubstrate (see lines 11-13).

Akram et al discloses a chip 12 having I/O pads 16. A polymeric material is attached to the chip, possibly using an adhesive (paragraph 0052). Note that this attaching of the substrate 18 to the chip 12 is done prior to the opening of vias in the chip. See Fig. 2, and paragraphs 0051 and 0054.

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It is agreed that Fanworth teaches a molding material of epoxy resin. However, the combination of Akram et al and Fanworth does not teach or suggest the detailed process of Applicants' invention wherein vias are opened in the adsubstrate to correspond to I/O pads on the chip followed by attaching the chip to the adsubstrate wherein the vias align with the I/O pads (Claim 11, lines 11-13).

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 11-13, 15, 17, 19, 20, and 22-25 as being unpatentable over Akram et al in view of Fanworth is requested in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 21 as being unpatentable over Akram et al and Fanworth in view of Yamamoto et al is requested in accordance with the following remarks.

As discussed above, the combination of Akram et al and Fanworth do not teach or suggest Applicants' detailed claimed process. The addition of Yamamoto et al, relied on for the temperature of attachment under pressure, does not teach or suggest Applicants' invention.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 21 as being unpatentable over Akram et al and Fanworth in view of Yamamoto et al is requested in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 42-51 as being unpatentable over Akram et al and Fanworth and Yamamoto et al is requested in accordance with the following remarks.

As discussed above, the combination of Akram et al and Fanworth does not teach or suggest the detailed process of Applicants' invention. The addition of Yamamoto et al, relied on for the temperature of attachment under pressure, still does not teach or suggest Applicants' invention. In Applicant's invention, vias are opened in the adsubstrate to correspond to I/O pads

on the chip followed by attaching the chip to the adsubstrate wherein the vias align with the I/O pads (Claim 42, lines 10-13).

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 42-51 as being unpatentable over Akram et al and Fanworth and Yamamoto et al is requested in accordance with the remarks above.

Allowance of all Claims is requested.

It is requested that should Examiner Owens not find that the Claims are now Allowable that he call the undersigned at 765 453-0866 to overcome any problems preventing allowance.

Respectfully submitted,

Rosemary L. S. Pike. Reg # 39,332